UNITED STATES PATENT AND TRADEMARK OFFICE

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SUN MICROSYSTEMS, INC. c/o DORSEY & WHITNEY, LLP
370 SEVENTEENTH ST.
SUITE 4700
DENVER, CO 80202

EXAMINER
SANDOVAL, PATRICK

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-25,28 and 30-42, wherein claims 4-5 and 26-27 are cancelled* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-3,6-16,18-25,28,30-34 and 36-42* is/are rejected.
7)☒ Claim(s) *17 and 35* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

1.   This Office Action responds to Applicant's amendment and drawing filed on 1/9/2008. Claims 1, 12, 15, 22, 30, 33, 37 and 40 have been amended. Claims 4-5 and 26-27 have been cancelled. Claims 1-3, 6-25, 28 and 30-42 are pending.

Continued Examination Under 37 CFR 1.114

2.   A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/9/2008 has been entered.

Response to Amendment

3.   Applicant's arguments, see Remarks pages 8-9, filed 1/9/08, with respect to the rejection(s) of claim(s) 1, 12, 22, 30 and 37 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly discovered prior art reference Limqueco et al. (Limqueco) (US 6,672,776). Applicable rejections are incorporated herein.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-3, 6-16, 18-25, 28, 30-34 and 36-42 are rejected** under 35 U.S.C. 102(e) as being anticipated by Limqueco et al. (Limqueco) (US 6,672,776).

6. **Pursuant to claims 1, 22 and 37**, Limqueco discloses:

receiving a circuit block netlist (Col. 3, II. 54-67 – Col. 4, II. 1-53);

obtaining a first estimated timing response of a first circuit path of said circuit block netlist using a first timing model (Col. 2, II. 56-67 – Col. 3, II. 1-10, Col. 4, II. 4-67 – Col. 6, II. 1-21, technology-independent critical path delay);

obtaining a second estimated timing response of a first circuit path of said circuit block netlist using a second timing model (Col. 2, II. 56-67 – Col. 3, II. 1-10, Col. 4, II. 4-67 – Col. 6, II. 1-21, technology-mapped critical path delay);

generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response (Col. 2, II. 56-67 – Col. 3, II. 1-10, Col. 4, II. 4-67 – Col. 6, II. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor); and

applying the correction factor to the first timing model (Col. 2, II. 56-67 – Col. 3, II. 1-10, Col. 4, II. 4-67 – Col. 6, II. 1-21, wherein the scale factor is applied to the technology independent, unmapped network).

7.   **Pursuant to claims 2, 23 and 38**, Limqueco discloses comprising obtaining estimated timing responses of a plurality of circuit paths using the first timing model (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein Limqueco discloses producing estimated delays).

8.   **Pursuant to claim 3, 24, 25 and 39**, Limqueco discloses selecting the first circuit path from the plurality of circuit paths, wherein applying the correction factor to the first timing model includes adjusting the estimated timing responses of the plurality of circuit paths based on the correction factor (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor, which is then applied to the technology independent, unmapped network).

9.   **Pursuant to claims 6, 28 and 41,** Limqueco discloses wherein generating a correction factor includes comparing the first estimated timing response and the second estimated timing response (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor).

10.   **Pursuant to claim 7 and 42,** Limqueco discloses wherein applying the correction factor includes adjusting the first estimated timing response based on the correction factor (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the scale factor is applied to the technology independent, unmapped network).

11.   **Pursuant to claim 8,** Limqueco discloses wherein the first estimated timing response includes an estimated signal propagation delay (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, estimated path delay).

12.   **Pursuant to claim 9,** Limqueco discloses wherein the first estimated timing response includes an estimated signal propagation time (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, estimated path delay).

13.   **Pursuant to claims 10 and 20**, Limqueco discloses wherein the correction factor includes a scaling factor (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor).

14.   **Pursuant to claims 11 and 21**, Limqueco discloses wherein the correction factor includes an offset (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor that offsets the overall estimated delays of the technology independent network).

15.   **Pursuant to claims 12 and 30,** Limqueco discloses:

obtaining coarse estimated timing responses for a plurality of circuit paths of a circuit block netlist using a first timing model, the first timing model having a first accuracy (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, technology-independent critical path delay);

obtaining refined estimated timing responses for one or more selected circuit paths of the plurality of circuit paths of said circuit block netlist using a second timing

model having a second accuracy greater than the first accuracy (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, technology-mapped critical path delay);

generating a correction factor based on the coarse estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the technology-mapped critical path delay is divided by the technology-independent critical path delay to obtain a scale factor); and

adjusting the coarse estimated timing responses of the plurality of circuit paths based on the correction factor (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein the scale factor is applied to the technology independent, unmapped network).

16.   **Pursuant to claim 13 and 31**, Limqueco discloses wherein obtaining the coarse estimated timing responses includes estimating timing responses for the plurality of circuit paths using a modeling tool employing coarse timing assumptions (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein Limqueco discloses producing estimated delays of technology independent networks).

17.   **Pursuant to claim 14 and 32,** Limqueco discloses wherein obtaining refined estimated timing responses includes using a modeling tool employing refined timing assumptions (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein Limqueco discloses producing estimated delays of technology mapped networks).

18.   **Pursuant to claims 15, 33 and 40,** Limqueco discloses comprising generating a netlist describing the plurality of circuit paths (Col. 3, ll. 54-67 – Col. 4, ll. 1-53).

19.   **Pursuant to claims 16 and 34**, Limqueco discloses wherein generating a correction factor includes determining a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths in the generation of a correction factor (Col. 3, ll. 43-52, wherein applied technology libraries statistically vary in process, feature sizes, performance, etc.).

20.   **Pursuant to claims 18**, Limqueco discloses wherein the coarse estimated timing responses include an estimated signal propagation delay (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, wherein Limqueco discloses producing estimated path delays for technology independent networks).

21.   **Pursuant to claims 19**, Limqueco discloses wherein the coarse estimated timing responses include an estimated signal propagation time (Col. 2, ll. 56-67 – Col. 3, ll. 1-10, Col. 4, ll. 4-67 – Col. 6, ll. 1-21, estimated path delay).

22.   **Pursuant to claim 36**, Limqueco discloses wherein the computer readable medium is selected from a group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, and an optically encodable disk (Col. 3, ll. 29-42, wherein a RAM, ROM magnetic tape, etc. are inherent to a computer readable medium).

Allowable Subject Matter

23.   **Claims 17 and 35** contain allowable subject matter.

24.   **Claims 17 and 35** objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

25.   The following is a statement of reasons for the indication of allowable subject

matter:

26.   **Pursuant to claims 17 and 35**, in a method of designing, analyzing and

comparing timing models, and a computer readable medium product for performing the

method, the prior art does not fairly teach or suggest:

        generating a correction factor for each of the plurality of circuit paths, wherein the

statistical variation is equal to a standard deviation of the correction factors for the

plurality of circuit paths divided by mean of the correction factors for the plurality of

circuit paths; and

        adjusting the coarse estimated timing responses of each of the plurality of circuit

paths individually, if the statistical variation exceeds twenty percent.

Remarks

27.   The objections to claims 1, 12, 22, 30 and 37 have been removed in light of

Applicant's amendment filed 1/9/2008.

Conclusion

28.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Patrick Sandoval whose telephone number is 571-272-

7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through

Friday.

29.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

30.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jack Chiang/
Supervisory Patent Examiner, Art Unit 2825

/Patrick Sandoval/

Examiner, Art Unit 2825